PRELIMINARY

Technical Information Manual

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MOD. V1729A
4 CHANNEL/14BIT
SAMPLING ADC
MANUAL REV.3

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1. Description of V1729A board

1.1 Generalities. Description of the overall functionality

The V1729A board is suited for acquisition of fast analog signals based on the MATACQ (analog matrix) chip [1] developed by collaboration of the CEA/DAPNIA and the l'IN2P3/LAL. This board, in the mechanical format 1-unit wide VME 6U board, is compatible with several standards of acquisition (VME A32/D64, A32/D32, A24/D16, GPIB and USB 2.0).

It is an evolution of the 12-bit dynamic range board series, and is compatible with the latter at power-up: it thus can be used by default with the same software.

It performs the coding of 4 analog channels of bandwidth tunable up to 300MHz over 14 bits at a sampling frequency (Fe) tunable up to 2GHz and over a depth of 2520 usable points. The channels can be grouped if needed in order to increase the sampling depth.

The measurement is realized in three phases (see Fig 1.1):

- **Acquisition** :
  the analog signal is continuously sampled at the frequency Fe in a circular analog memory. The arrival of a trigger signal initiates the stopping phase of the sampling, see 2.1.1. At the end of this phase, the state of the memory is set: it then contains the last 2560 points sampled (out of which 2500 are valid).
- **Conversion and storage** :
  after a stopping order of the acquisition, the samples stored under analog form in the MATACQ chips are rapidly (650µs) re-read and coded into digital data over 14 bits, then stored in a digital memory buffer. The acquisition is informed of the end of the coding phase either by scanning of an internal register, or by an interruption.
- **Reading** :
  the memory buffer can then be re-read by the acquisition system. For an acquisition system of VME A24-D16 standard, the latter operation lasts a few ms for the full readout of a 4-channel board, which permits attaining an acquisition frequency of a few hundred Hz for the acquisition of 2500 points per channel. With a high performance A32-D32 system, one should pass 500Hz, and approach the kHz with a performing A32/D64 system.

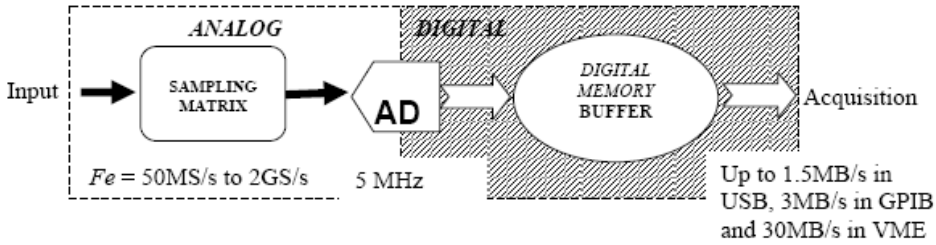


Fig. 1.1: data flow in the board

1.2 Sampling frequency

The V1729A board is sequenced by an oscillator at a frequency of 100MHz. No greater frequency signal exists on the board. This is what explains the low consumption of the system. The sampling at a very high frequency (Fe) in the MATACQ chip is in fact realized by virtual multiplication of frequency inside the chip by a factor up to 20.

The MATACQ chip functions with a pilot frequency of 50MHz or 100MHz programmable on the board by software, which corresponds to a sampling frequency Fe (= 20*Fp) of 1 or 2 GHz. The EXT_CLK input may possibly be used to inject a very clean external pilot clock comprised between 50MHz and 100MHz. **Caution**: the MATACQ chip cannot work properly with a pilot frequency Fp lower than 50MHz.

1.3 Input signals & Dynamic range

The V1729A board integrates 4 analog channels. Depending on the different versions, the inputs of these channels are connected through simple LEMO plugs (IN0 to IN3), double (IN0± to IN3±), or SMA plugs (IN0 to IN3).
The inputs are by default unipolar and terminated on 50 Ohms. However, the input levels of the board can be very easily modified (through displacing a few resistors and mounting new ones) in such a way as to permit the input in differential mode (from which the possibility of mounting double LEMO plugs). For this purpose, free CMS-805 resistor footprints are indeed implemented on the V1729A board (see section 4).
The analog to digital conversion is made on 14 bits with a maximum dynamic range of 2V, or an LSB of 125µV. This range is centred on 0V (± 1V). However, free CMS-805 footprints are implemented on the V1729A board for shifting the dynamic range in the interval ± 0.5V in order to be able to optimize the system for unipolar signals (see 4.1.8).
The measured noise referred to input is less than 175 µV RMS, and the integral non-linearity remains below 1 per 1000 over the whole dynamic range.

2. Mode of operation

2.1 Definition of the acquisition window & Trigger modes

2.1.1 Principle, PRETRIG, POSTTRIG

During the acquisition, the analog signal is continuously sampled in the analog memory which is comparable to a circular buffer with a depth of 2560 points (time depth = 2560/Fe). The stopping of sampling is initiated by the arrival of a trigger signal *Ta (asynchronous trigger)* which is common to all the channels of a board. This signal is only authorized to be produced following a programmable delay named *PRETRIG* after the triggering of the acquisition sequence.

The effective stopping of the sampling will occur following a pre-defined number (named *POSTTRIG)* of clock periods (50MHz or 100MHz) after the trigger (see Fig 2.1).

The *POSTTRIG*, programmable by the user, permits defining and displacing the position of the trigger signal in the acquisition window. It is adjustable in the 1/Fp to 65535/Fp range by steps of 1/Fp (= 20ns or 10ns), to which a fixed extra offset of 7/Fp has to be added. This is illustrated in Fig 2.2.

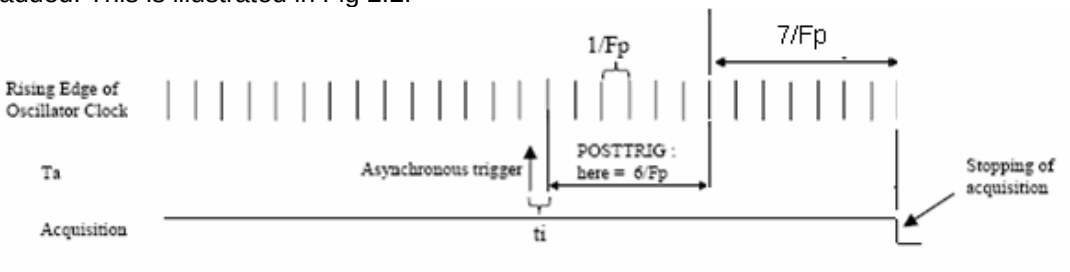


Fig. 2.1: chronogram of the stopping of the acquisition

In the example illustrated by Fig 2.1, the total POSTTRIG is fixed at 13/Fp (6/Fp programmed in the register + 7/Fp extra offset). The acquisition will be stopped 13/Fp + ti after the arrival of the trigger signal (ti corresponds to the time measured by the vernier between the Ta and the next rising edge of the clock – see 2.4.2). The analog memory will then contain the 2560 last recorded samples (of which only the last 2520 after re-alignment will be exploited).

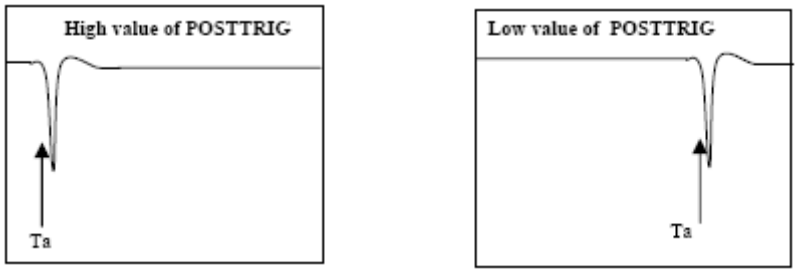


Fig. 2.2: centering of the Trigger in acquisition window for two POSTTRIG cases

Thus, a POSTTRIG value close to 64 assures the centering of the trigger in the middle of the acquisition window. For the values of POSTTRIG > 118, the trigger position no longer appears in the acquisition window.

2.1.2 Trigger sources

There exist four possible sources for the trigger signal Ta. They are selectable by the user (see 4.4):

- **Trigger on signal** : this is the result of the logic « OR » of the discriminators on the analog signals of one or several channels of the board by choice of the user. The individual thresholds of the discriminators are programmable by steps of 0.5mV (12-bit DACs) over a range of ± 1V (which corresponds to the integrality of the usable input range of the board). The user can also define the type of discrimination (signal crossing the threshold upwards or downwards) via the choice of the trigger edge.

- **External trigger** : external trigger signal entering on a LEMO plug (EXT_TRIG signal at the NIM level). This signal can be either used as any other trigger source with choice of its edge, or exploited directly as an asynchronous trigger (rising edge only) in cases where one uses discriminators from several boards in order to produce at the exterior of the boards (via their output TRIG_OUT) a trigger which will be sent back to them in a synchronous way (see figure 2.3). This mode is selected by the bit 4 of the TRIG_TYPE register (see 4.4).

- **Auto trigger** : triggered by a software command issued from the acquisition. It permits the generation of a random trigger. This corresponds to the automatic trigger mode.

- **« Auto + normal » trigger** : result of a logic « OR » between the trigger on signal and the automatic trigger.

- **Internal random trigger** : this internal periodic signal is asynchronous from the clock. When it is selected and the trigger mode chosen is « auto », this signal serves as a source for the automatic trigger. One uses it for the fast calibration of the verniers of the MATACQ chips (see 3.3.1).

2.1.3 Trigger edge

The trigger edge (rising or falling) can be selected in all modes (except the direct external trigger which uses only the rising edge).

2.1.4 TRIGOUT signal

A copy of the pre-trigger signal (positive pulse) generated by the V1729A board is available at the output on a LEMO plug on the front panel (TRIG_OUT output on the NIM level). It can in particular permit synchronization of trigger for several boards.
A simplified summary of the trigger modes of the board is presented in figure 2.3.

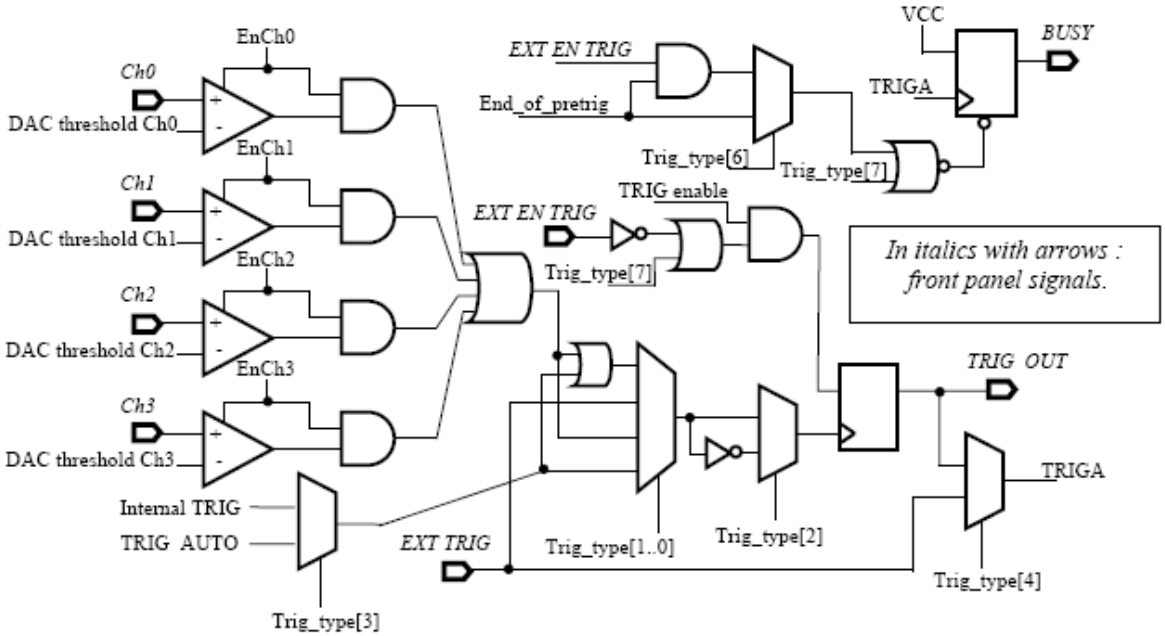


Fig. 2.3: simplified description of the trigger selection chain

2.1.5 Validation of the trigger by a second subsequent signal

In the case where one would like to validate the data stored in the MATACQ chips before their transfer towards the RAM, it is possible to make use of the *EXT_EN_TRIG* input to introduce there through a validation signal (see figure 2.4). This is particularly useful if the system produces such a signal with a delay greater than the maximum sampling depth (2560/Fp i-e 1.25µs at 2GS/s and 2.5µs at 1GS/s) and smaller than the transfer time towards the RAM (675µs). This can thus permit a big decrease of the potential dead-time linked to the readout. In this case, the usual use of the *EXT_EN_TRIG* signal (which permits inhibiting the trigger as described on figure 2.3) is inhibited.

In order to perform the validation, a programmable 8-bit latency counter (called POST_STOP_LATENCY) with steps of 2.5µs is started at the end of the POSTTRIG, and if the external validation signal hasn't arrived before the end of that delay, the Matacq chips switch back into the analog input signal writing mode thus waiting for the next trigger. If on the other hand the validation signal did arrive, the waiting data is digitized then stored into the RAM. This mode is validated thanks to the bit 5 of the TRIGGER_TYPE register (see 4.4). Moreover, a second 8-bit register (called POST_LATENCY_PRETRIG) with the same steps of 2.5µs permits the programming of the time to wait before enabling the trigger again if the validation didn't occur. The minimum time for refilling is of 1.25µs at 2GS/s and of 2.5µs at 1GS/s. The minimum value in that register is thus 1.

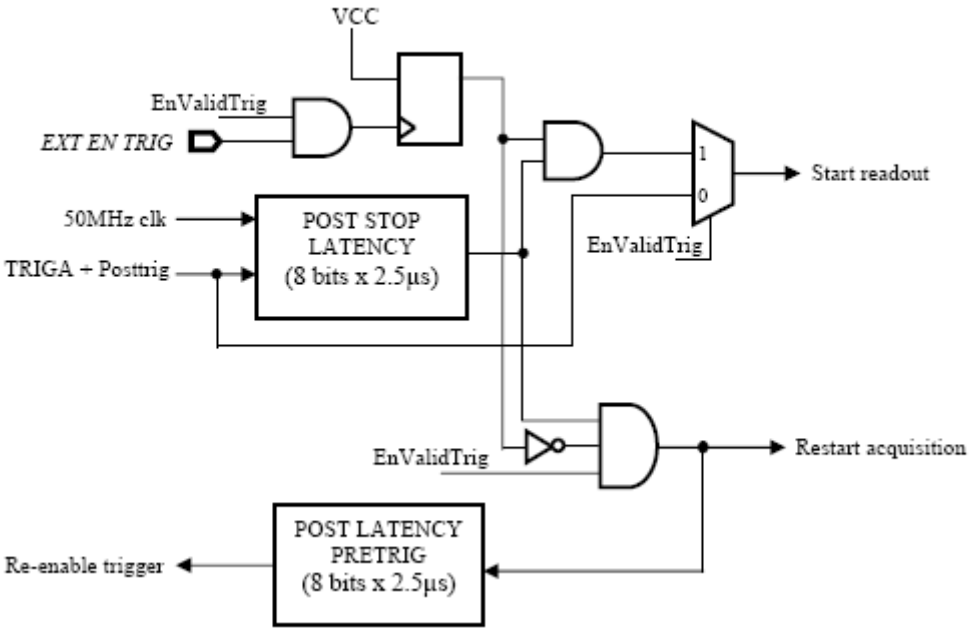


Fig. 2.4: simplified description of the trigger validation system

2.2 Dead time at the start of the acquisition; Pretrig

The frequency of the clock present on the board is relatively low (50MHz or 100MHz). In order to be able to sample at a rate equal to or greater than the Giga-sample per second, the MATACQ chips realize a virtual multiplication of frequency. This multiplication requires a servo of which the control loop is interrupted at the time of the data read cycle. At the time of the start of the acquisition, this servo has to get locked again. This implicates a typical waiting of 150µs before being able to reach the optimum of the sampling performances.
For this reason, at each restarting of the acquisition, the board must automatically generate a dead time during which the triggers are not accepted.
This dead time is adjustable by the PRETRIG, from 1 to 65535 times the period of the main clock. The recommended PRETRIG values are therefore :

- 7500 (decimal) for a clock frequency of Fp = 50MHz.
- 15000 (decimal) for a clock frequency of Fp = 100MHz.

2.3 Standard acquisition sequence

2.3.1 Acquisition started by user

Fig 2.4 shows the standard course of an acquisition :

- The sequence begins with the initialization of the board by a *RESET* order.

- Next, the different parameters which are not used with their default value must be programmed (PRETRIG, POSTTRIG, TRIGGER TYPE, TRIGGER EDGE, MASK, NB OF COL TO READ, FP FREQUENCY, …).
- The starting order of the acquisition is next sent (START_ACQUISITION). The latter can also be generated automatically (see 3.3.2).
- The user if necessary sends a software trigger (in the case of an automatic trigger) having taken care to wait at least the time necessary for the PRETRIG.

- The program then waits for a request emitted by the V1729A board when the data are ready to be read. For this, there exist two possibilities illustrated by Fig 2.5 :

- Waiting and handling of an interruption (SRQ in GPIB, IRQ1 to 7 in VME, specific format in USB).
- Regular scanning of the LSB of the interruption register (INTERRUPT h80).

The first solution has the big advantage of being less noisy for the front-end of the board for it does not require any bus access. In both cases, the user should acknowledge the request by writing a 0 in the *INTERRUPT* register, but the latter is anyhow reset by the START_ACQ command.

- The user can then partially or wholly read the data stored in the board. This includes :

- the values of the vernier and of the samples (see 3.3.1)
- the value of TRIG_REC which permits determination of the position of the trigger in the acquisition window (see 4.3.2)

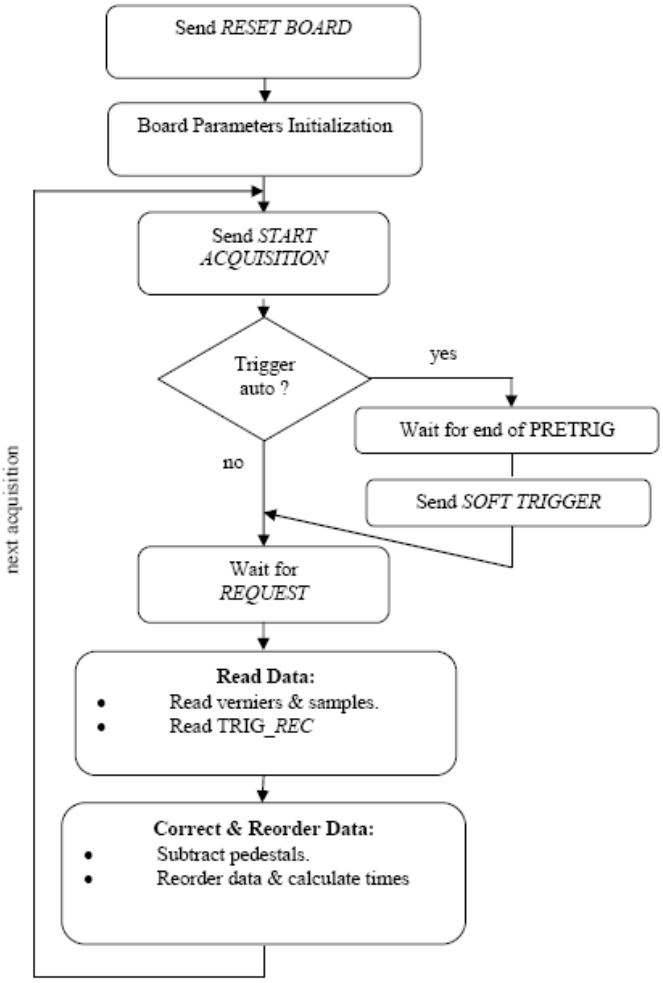


Fig. 2.5: block diagram of a standard acquisition

- The user must correct the data before using it (see 2.4):
  - By subtracting the pedestals (see 2.1.1).
  - By reordering the data (see 2.4.2).

  These operations can be executed on-line or off-line according to the context.

2.3.2 Automatically restarted acquisition

In order to reduce the dead-time due to the restarting of the acquisition, an automatic mode has been implemented on the board. Its use is conditioned to the bit 2 of the MODE_REGISTER (see 4.4) which is set to 0 by default. The working principle is the following :
when this bit is set to 1, one has to perform the first acquisition in a usual way via the START_ACQUISITION command. At the end of the latter, it is necessary to read at least one of the three registers TRIG_REC, Valp_cp and Vali_cp **in the RAM** (see 4.3.2). During the reading in the RAM of any of those, a START_ACQUISITION command is generated automatically. Caution : if one wants to read the three of them, one disposes then of the PRETRIG duration to read the two last ones. Reading the RAM after the end of the PRETRIG may indeed pollute the analog data of the new starting acquisition sequence.
In order to leave this mode, one just has to reset the bit 2 of the MODE_REGISTER.

Caution : one has to take care of not « forgetting » the board running in this mode without trigger occurring for it then remains blocked in acquisition state, thus with the maximum power consumption.

2.4 Correction of data

The raw data extracted from the board must be treated before really being usable. This treatment consists of two operations :

- Correction of the pedestals.
- Reordering and time alignment of the data.

2.4.1 Correction of the pedestals

The analog memories of the MATACQ chips present by design dispersions of pedestal from cell to cell which can reach several tens of mV. On the other hand, the pedestal of a data cell is extremely reproducible (250µV RMS). Due to the structure of the chip, the dispersion of the pedestals presents a principal periodicity of 20 cells, followed by a tiny individual distribution. If not compensated, this dispersion will appear as a noise at the reconstruction of the signal because of the random position of the trigger in the matrix.

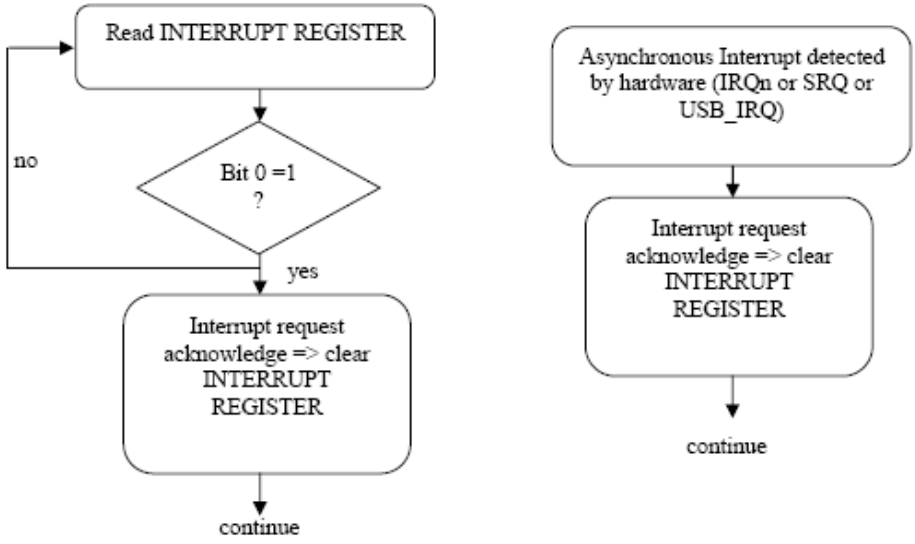


Fig. 2.6: scanning of interruption register or treatment of asynchronous interruption

In order to obtain the nominal noise performances (signal to noise ratio of 81dB), the pedestals, which are stable in time and with temperature, must be removed by the acquisition software individually cell by cell. As discussed above, it is also possible to subtract 128 times a pattern of 20 cells. This makes it possible to store only 20 pedestals, and the loss of the signal over noise ratio remains minor (approximately 1 to 2dB) even though it is not negligible.
Since the pedestal of a cell is linked to its physical location and not to its position in relation to the Trigger, **it is necessary to realize this removal BEFORE reordering the data**.

A method of calibration of the pedestals is demonstrated in section 3.3.

2.4.2 Temporal corrections

The signal is sampled in a circular memory. The first operation necessary for the treatment of the data is therefore to « unfold » the circular memory of every channel in order to obtain tables of 2560 temporally ordered data (see Fig 2.7). This can be done, by example, by realizing a rotation of :

(1) ROT = (*TRIG_REC - POSTTRIG*) * 20

cells towards the left of the data tables issued from the RAM and formerly sorted channel by channel (see 4.3).

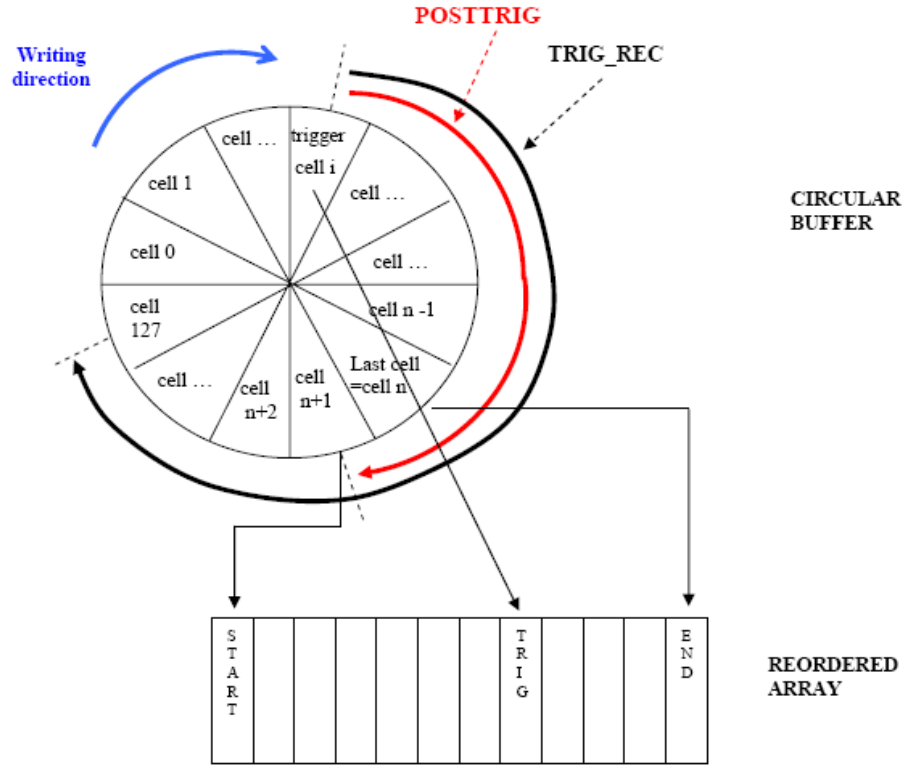


Fig. 2.7: unfolding of the circular memory

Or, equivalently through a calculation of a new index number for each data :

(2) NEWi = (2560 + OLDi – END_CELL) modulo 2560

where END_CELL is the index of the last written cell :
END_CELL = 20 * (POSTTRIG +128- TRIG_REC) modulo128

The trigger signal TRIGA (asynchronous trigger) is the absolute reference which serves to temporally realign the data (see Fig2.1). In order to find its position, one uses the information provided by a temporal interpolator (vernier) measuring ti, time interval separating the arrival of TRIGA from the next rising edge of the Fp clock.
This information associated with the *MINVER* and *MAXVER* calibration constants (see 3.3.2) permits determination of the position of the Trigger and therefore realignment of the data with a typical maximum precision in the region of 50ps RMS. This realignment is unnecessary if the user simply desires to study the signal shape and in this case, the curve acquired will present a jitter of a period of Fp. The information of the 4 verniers from the same board being redundant in order to realize the temporal adjustement, it is therefore possible:

- to use solely the vernier from the channel 0.

- to use the vernier i for the channel i.
- to calculate the mean of the 4 verniers in order to refine the time precision.

The following formula permits determination of the time of each point of the reordered table, with by convention a time origin (Time = 0) at the arrival of the Trigger.

(3) Time[NEWi] = DT0 + {NEWi - 20 *[128 - POSTTRIG + Correc_Ver]} * dT

With (4) Correc_Ver = (VERNIER - *MINVER*) / (*MAXVER* - *MINVER*)

Where :

- dT is the sampling period (500ps or 1ns)
- DT0 is a fixed temporal offset, close to 0, due to signal propagation times in the board (of which the calibration is described in 3.1.1

An alternative but equivalent solution, consists in generating the reordered table through a rotation towards the left of the data of :

(1b) ROT = (*TRIG_REC* - *POSTTRIG*) * 20 – INT(Correc_Ver*20) *cells where INT corresponds to rounding off to the nearest whole number.*

The trigger is then situated at a time

(5) tT= [**Correc_Ver*20– INT(Correc_Ver*20)]* dT**

before the cell numbered 20(128-POSTTRIG) (plus the offset DT0).*

2.5 Functioning with two 5k or one 10k-channel

The V1729A board permits grouping either 2 x 2 or the 4 channels of the board in order to increase the sampling depth. One then has to inject the same signal into the front panel on the inputs of the concerned channels. In this case, a complement of POSTTRIG will be added automatically in order to fill up the supplementary depth. It will depend on the number of grouped channels and of the chosen sampling frequency Fe. Trigger will always be located within the first 2520 points or before (depending on the POSTTRIG).

Grouping of channels	POSTTRIG in samples	POSTTRIG in time
4 x 1	Normal (as programmed)	Normal (as programmed)
2 x 2	Normal + 2520	Normal + 2520/Fe
1 x 4	Normal + 3 x 2520	Normal + 3x2520/Fe

There may be a slight difference in time and in gain between channels. In order to calibrate the gain difference, a continuous voltage set at the three quarters of the full scale for both polarities is recommended. Concerning the time offset, a calibration using a voltage ramp might be necessary. The last points of the first channel will be compared to the first of the following one, and so on if more than two channels are concerned.

3. Synchronizations, calibrations, monitoring

3.1 Synchronization between the channels

3.1.1 Channels from the same board

A single trigger signal is used for all of the channels from the same board. The acquisition of these channels will therefore naturally be synchronous, with a typical jitter of only 20ps RMS. The possible temporal offset dT0, constant, between the channels (principally due to the propagation of the trigger signal on the board, but also to the different lengths of cables at the inputs) will be calibrated once for all. This calibration is executed by sending a same signal on all of the inputs and by looking for the fine position of the trigger on each of the channels.
In the case where the board is triggered on one of the input signals, a fine synchronisation method consists of interpolating by software the crossing of the signal through the trigger threshold on the given channel, this permitting the fine datation of all the measured channels.

3.1.2 Channels situated on different boards

The synchronization is only possible if the trigger source is common to the different boards. For this, several possibilities can be envisaged :

- to use an external trigger signal common to all of the boards.
- to generate the trigger signal on a fixed board (master) which triggers itself and to send its TRIG_OUT signal output to the external trigger input of the other boards (via a NIM buffer if there is more than one target board).
- to generate the trigger signal on any one of the boards. The TRIG_OUT outputs of all of the boards will then be connected on an external NIM logic then the result will be redistributed in a synchronous fashion to all the boards via their EXT_TRIG input. It is this latter input which will then be programmed as the source of the asynchronous trigger via the bit 4 of the TRIGGER_TYPE register on all the boards.

In all cases a calibration of the temporal offset between the boards is necessary. This calibration, similar to that which is necessary to align the channels from the same board, will be dependent upon the set-up (length of the cables…).

3.2 SYNC_OUT and BUSY signals. Partial reading of matrices

One of the NIM outputs of the front panel can be configured either as a SYNC_OUT, or as a BUSY respectively with the help of the S4 and S2 straps. SYNC_OUT is a synchronization signal corresponding to the writing in the first cell of the second column of the circular analog memory, and which can be made available on the front panel. For certain applications, this signal can permit triggering of the source analog signals and thus guaranties their fixed position in the memory. Thus, if the temporal occupation of the signals to acquire is low, the user will have the possibility to only re-read the beginning of the depth of the analog memory and to thus limit the dead time linked to the acquisition.

BUSY is a signal destined to inform the external world that the board is not ready to receive a signal (it is either idle, or in the process of transferring data between the MATACQ chips and the RAM, or at the beginning of the acquisition phase). Its transition to 0 indicates then that the board is now ready to record a signal.

3.3 Calibrations

In order to attain the optimal metrological performance, the V1729A board requires calibrations. These remain valid for several weeks, even several months. The corresponding data can thus be memorized for each acquisition mode. To this end, a 128kBytes EEPROM is available on the board.

3.3.1 Calibration of the interpolator

The temporal interpolator (vernier) requires a calibration. This operation will be necessary following **all changes** in the sampling frequency. Once performed, its result will be able to get stored and re-used. This calibration, based on a statistical measure, will require the acquisition of several thousand events and can last from one second to a couple of minutes depending on the type of bus and on the software used. It can be done with the inputs connected to any source, but the trigger must be asynchronous in relation to the clock. The result of this calibration will be a “square” histogram, of which the sides correspond to two successive rising edges of Fp. The corresponding value on the left side (*MINVER*) will be the « zero » of the vernier, and the one on the right side (*MAXVER*) will correspond to a vernier of 1/Fp (in other words 10 or 20ns). The intermediate values will next be deduced at the time of the acquisitions by a simple proportional calculation.
The most precise but the longest calibration method consists in putting the system in the mode (TRIGGER_TYPE, PRETRIG, POSTRIG) which will be used for real measurements, and in accumulating a few thousands of events until the edges of the vernier distribution be well drawn. The precision obtained will then be the highest but many minutes might be necessary.

If a lower precision is sufficient, faster modes do exist. The diagram in Fig 3.1, which follows from that in Fig 2.4, indeed shows the sequencing of such a calibration, optimized so as to be the fastest possible. In particular :

- The PRETRIG and POSTTRIG are fixed at their minimal value.
- NB_OF_COL_TO_READ has to be set to 1.
- Only the vernier values are read in the RAM. In other words, if NCH channels are read, only the 2*NCH first data are read and only the NCH+1 to 2*NCH words are conserved (see 4.3).

After a certain number of acquisitions (at least 10000), the boundaries of the vernier *MINVER* and *MAXVER* can be calculated.

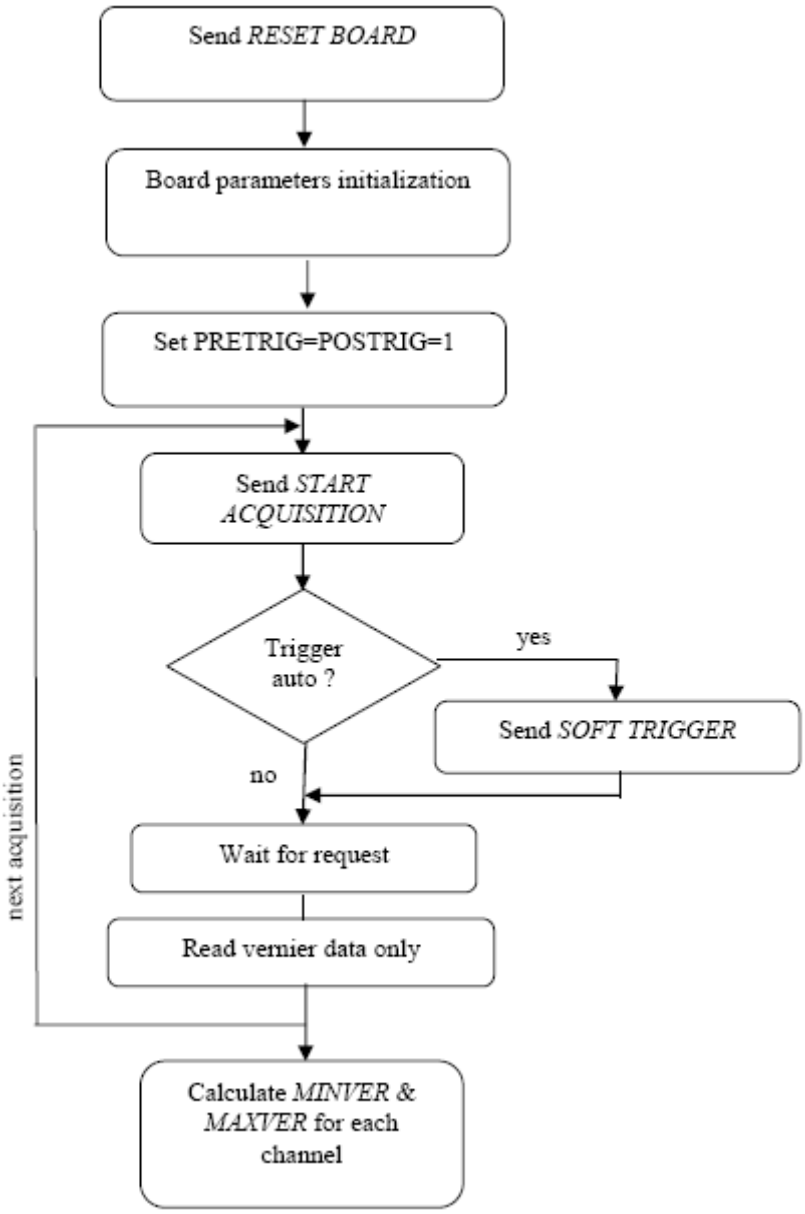


Fig. 3.1: diagram of the calibration of the verniers

At first approximation, it is possible to simply use the minimal and maximal values of the vernier for *MAXVER* and *MINVER*. This method is sufficient to obtain temporal resolutions in the region of 70ps RMS.
To get greater precision, one must in order to find the two sides fix a threshold corresponding to half the mean number of ADC counts in the « square » distribution.
To obtain even more precision, it is possible to use more complex methods.

A second, much faster method of calibration is available. For this :

- Charge NB_OF_COL_TO_READ at 0.
- Position the trigger in auto mode.
- Validate the internal random trigger.
- Launch a Start_ACQUISITION.

The RAM is then filled with 65536 vernier values corresponding to 16384 random triggers. For each trigger one finds only 4 values, arranged in the following order :
Channel 3 vernier, channel 2 vernier, channel 1 vernier, channel 0 vernier.
At the end of this calibration, an interruption is generated in order to permit the user to launch a reading. This reading can be realized in block mode, which permits realization of the calibration of the vernier in less than one second if the PRETRIG and POSTRIG are short.
One must note that for this particular method of calibration, the distributions obtained are not necessarily uniform. Nevertheless, the MAXVER and MINVER boundaries are extremely well-defined and therefore perfectly exploitable for corrections. If ever this weren't the case, it would be necessary to run the calibration again but with a different value of PRETRIG.
In order to improve the precision, it is also possible to perform this operation a few times in a row, thus accumulating more data in the histogram.
Our experience showed us that this calibration remains valid several weeks, even several months. The boundaries can nevertheless be updated in real time from the readout event data if their triggering is random relatively to the board pilot clock.

3.3.2 Calibration of the pedestals

For this, a calibration of the baselines is necessary. This operation will be necessary following **all changes** either in the sampling frequency, or in the bandwidth of the write amplifier (BWL), or in the read modes (FAST READ MODES). It will consist in realizing a mean measurement over a few tens of raw acquisitions of the baselines for all of the cells. During this operation, the inputs must be:

- either disconnected,
- or grounded,
- or, and this is the best solution in term of rejection of parasitics, connected to their source with no signal or with the source not powered.

The trigger must then be either automatic, or external.
The acquisition procedure is the same as for a standard acquisition, but the reading of TRIG_REC can nevertheless be skipped. Of course not the least temporal correction is made on the data. At each acquisition, the table of the means will be computed and finally recorded for an eventual subtraction by software from the unaligned raw data. This calibration operation lasts less than one second.
In cases where the input is connected to unlikely physical signals, it is also possible to realize this calibration without disconnecting the input. However, it will then probably be necessary to increase the number of acquisitions in order to diminish the effect of the induced additional noise.
Our experience shows us that this calibration remains valid several weeks.

3.3.3 Temporal calibration between different channels

See section 3.1

3.4 Trigger rate monitor

The dead-time linked to data transfer towards the RAM and to the event readout doesn't allow the user to know about the actual trigger rate of the board in the conditions defined for the trigger. This is the reason why the V1729A board offers the possibility to measure

directly this rate thanks to two counters called “trig_count” and “time_count”. The first one counts the number of triggers produced in the current defined trigger conditions, whereas the second one counts the number of µs elapsed since the beginning of the counting. The lowest significant bit of the register called RATE_REG permits the counting. The latter, which functions up to 200MHz, starts upon TRIGA and stops:

- either upon the reading of any of the two counters,
- or when any of them saturates.

It is possible to read the four bytes of the counting registers in block mode and thus to gain a lot of time in USB for instance.

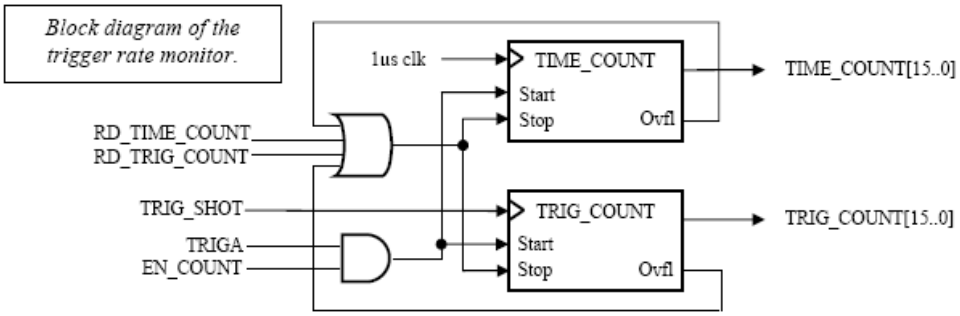


Fig. 3.2: Trigger rate monitor

4. Technical description

4.1 Mechanical and electrical standards

4.1.1 Mechanical standard

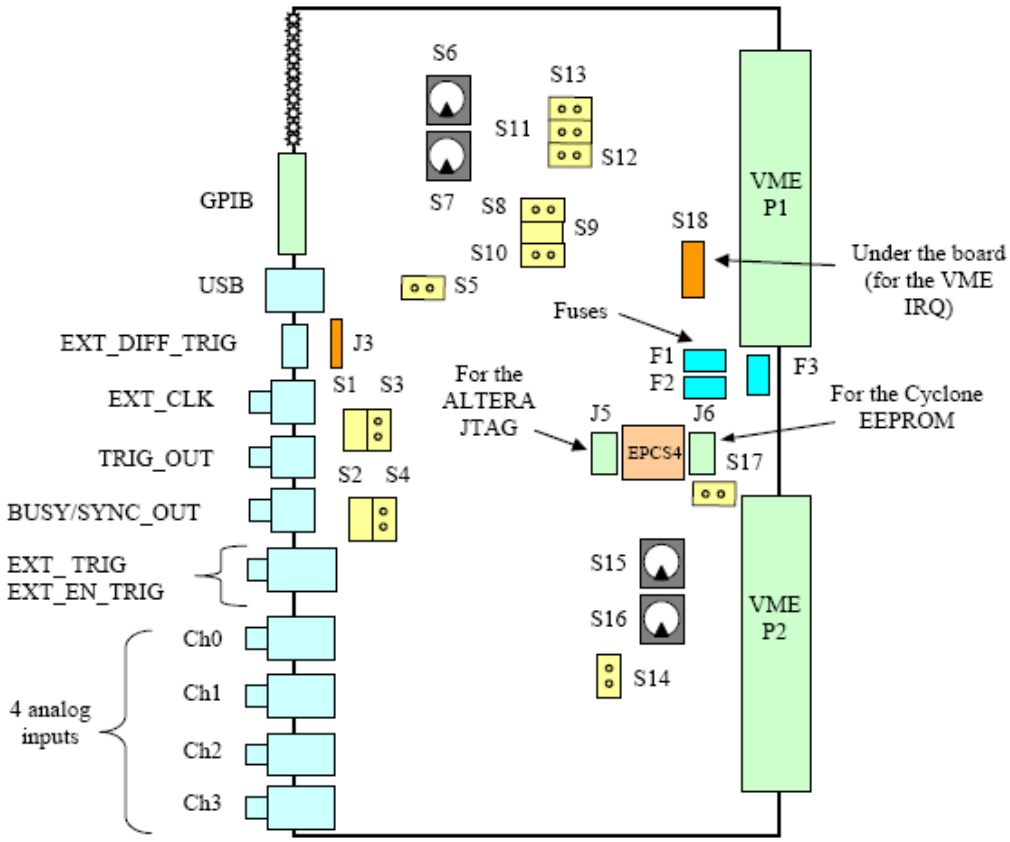


Fig. 4.1: connectors and configuration elements on V1729A

The V1729A board is of VME 6U (160x233,3mm2) mechanical format. The two connectors P1 and P2 of the VME crate are usable, both for the supply and the VME dialogue. However, these boards can completely be accessed via the USB and GPIB busses out of a VME crate, or by only using the latter as mechanical and power supply support.

The plugs used for all the digital inputs/outputs are of female LEMO type. The analog inputs are either in simple LEMO, in SMA, or in double LEMO, depending on the version.

4.1.2 Electrical interfaces

The V1729A board is compatible with three acquisition busses :

- VME via the P1 connector of the VME (plus the P2 for the A32/D32 mode), 96 pin male connector DIN 41612 .
- GPIB via the two-row connector located on the front panel (26 points male).
- USB 2.0 full speed (12Mb/s) via the B-type USB connector on the front panel.

This board has an address coded over 8 or 16 bits, configurable through a set of hexadecimal rotary switches. For the GPIB and the VME A24/D16, one uses only the two rotary switches S6 and S7. For the VME A32/D32 or A32/D64, one must also use the two rotary switches S13 and S14.

- In GPIB, the address is configurable from 1 to 29 (decimal).
- In VME, the address is configurable from h01 to hFF on the bits 16 to 23 for the A24/D16 mode, and from h0001 to hFFFF on the bits 16 to 31 for the A32/D32 and A32/D64 modes.

The choice of the type of interface is determined by the S9 and S10 jumpers. By default (without jumper), the bus used is the VME. When the jumper S9 is mounted, USB is used. When the jumper S10 is mounted, GPIB is used (if both: a specific reduced VME mode is selected).

4.1.3 Summary of front panel signals

The fast logical signals of input “EXT_TRIG” and of output “BUSY/SYNC_OUT” and “TRIG_OUT” of the V1729A board use the NIM standard (-16mA in 50 Ohms i-e -800mV for the logical state « 1 », no current i-e 0V for the logical state « 0 »).

Plug name	Purpose	Connector	I/O	TYPE
IN0+ to IN3 +	Positive Analog Inputs	Half double LEMO or SMA	I	50Ohm terminated
IN0- to IN3 -	*Negative Analog Inputs (option)*	Half double LEMO	I	50Ohm terminated
EXT_EN_TRIG	*External Trigger Enable*	Half double LEMO	I	NIM
EXT_TRIG	External Trigger	Half double LEMO	I	NIM
EXT_DIFF_TRIG	External Trigger	Double pin	I	DIFF ECL (adaptable by J3)
EXT_CLK	*External clock*	LEMO	I	NIM
TRIG_OUT	Trigger Output	LEMO	O	NIM
BUSY/SYNC_OUT	Busy/Synchro Output	LEMO	O	NIM

The front panel leds permit having an image of the current status of the board. The green ones show the presence of the external power supplies, whereas the red ones are linked to the internal signals via monostables which permit the visualization of very short pulses and to digital gates for the continuous levels.

Led name	Type	Function
VME	Monostable + gate	VME access acknowledged by the board.
GPIB	Monostable + gate	GPIB access acknowledged. Remains ON if no EOI is sent by the controller at the end of a writing sequence.
USB	Monostable + gate	USB access acknowledged by the board.
RESET	Monostable + gate	Board reset.
CLOCK	Monostable only	The Altera FPGA is providing the main clock to the board.
BUSY	Monostable + gate	Displays the BUSY signal.
ACQRUNNING	Monostable + gate	Is set ON after a “start acquisition” command. Is set OFF at the end of the POSTTRIG.
TRIG	Monostable + gate	Image of the TRIGA signal.
WR-RAM	Monostable + gate	Write access to the data RAM.
INTERRUPT	Monostable + gate	Displays the INTERRUPT signal which is produced at the end of the acquisition sequence.

4.1.4 Supplies

The V1729A board makes use of the standard supplies of the VME: ±12V and +5V.
It fabricates the –5V for the ECL logics starting from the +5V with the help of a DC-DC converter capable of delivering 600mA.
The 3.3V for the MATACQ chips is regulated from the +5V input. The -3.3V is regulated from a -5V produced in a second DC-DC converter capable of delivering 1A.
The intensities consumed on these different supplies are:

Supply	Consumption	Fuse	Calibre
+12 V	0.35A	F2	1A
-12V	0.15A	F1	1A
+5V	1.5A + X x Y x 1.2A	F3	5A

where X is the rate of acquisition = relation of time spent awaiting the event / total time .
X is worth 1 in the case of infrequent event acquistions.
X is low (can fall to 1%) in the case of frequent events. In this case indeed, the dead time for readout is dominant in relation to the time spent awaiting the event.
Y depends on the bandwidth mode (see control registers in 4.3.2) :

	BWL0	**BWL1**	**Bandwidth**	**Y**
Full bandwidth mode	0	0	300 MHz	1
Normal mode	1	0	230 MHz	0,6
Normal mode	0	1	230 MHz	0,6
Low power mode	1	1	180 MHz	0,35

4.1.5 Pinout of the non-standard connectors

GPIB Connector (two-row 26-pin male, pitch of 1.28mm, ERNI mini HE10 male B type)

Reference: J2.

1 : D1	2 : D5
3 : D2	4 : D6
5 : D3	6 : D7
7 : D4	8 : D8
9 : EOI	10 : REN
11 : DAV	12 : GND
13 : NRFD	14 : GND
15 : NDAC	16 : GND
17 : IFC	18 : GND
19 : SRQ	20 : GND
21 : ATN	22 : GND
23 : GND	24 : GND
25 : NC	26 : NC

The corresponding female connector can be directly pressed on a 24 wire flat cable equipped at the other extremity with a GPIB standard connector (CENTRONICS 24 points). Up to 18 female connectors can be mounted in parallel on the flat cable (then take care of the bus signal integrity).

- *Active Serial connector for the Cyclone ALTERA E2PROM* (10-pin two-row female, pitch of 1.28mm)

Reference: J6.

Permits reloading the ALTERA E2PROM (EPCS4) from an Altera file « .pof » in the so-called “active serial” mode.

- *JTAG connector for the two ALTERAs* (10-pin two-row female, pitch of 1.28mm)

Reference: J5.

Permits accessing the two ALTERAs directly through JTAG and reprogramming them.

4.1.6 Straps and resistor network sockets

A certain number of sockets for straps, switches and resistor networks are available on the board. These are their respective roles:

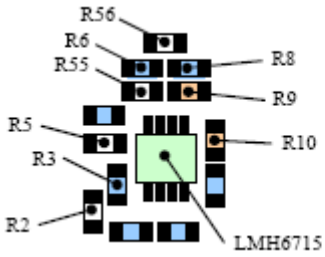
Reference	Role
S1	one utilizes the differential EXT_TRIG differential input (exclusive of S3)
S3	one utilizes the unipolar EXT_TRIG input by Lemo (exclusive of S1)
S2	the BUSY/SYNC_OUT output releases the BUSY signal (exclusive of S4)
S4	the BUSY/SYNC_OUT output releases the SYNC_OUT signal (exclusive of S2)
S5	To pull down the SI_WU input of the FT245B.
S6 and S7	address of the board (see 4.1.2)
S8	normally absent. Permits selecting EXT_SYNC as the main board clock.
S9 and S10	choice of the acquisition data bus (see 4.1.2)
S11	one utilizes the EXT_CLK input for the main clock (exclusive of S11)
S12	one utilizes the 100MHz oscillator for the main clock (exclusive of S10)
S13	sends the EXT_CLK signal towards the EXT_SYNC input of the ALTERA
S14	normally absent. Permits switching the output of the FT245B towards the JTAG bus in order to configure the ALTERAs and the Cyclone’s PROM via USB.
S15 and S16	address of the board (see 4.1.2)
S17	normally absent. Prevents the conf_done to rise which then permits not to validate the configuration of the Altera at power-up.
S18*	Choice of the VME IRQ (IRQ1 at the bottom to IRQ7 towards the top).
J3	adaptation for the EXT_DIFF_TRIG input. Place 100 ohms between the pins 1 and 2 and between the pins 3 and 4

* located under the board.

4.1.7 Implementation of differential inputs

The input signals are by default unipolar. In order to use differential inputs, one must make use of certain free CMS-805 resistor locations located close to the input amplifiers (LMH6715) and change some others. The equipment map of this zone of the board is presented below. The already present resistors appear in blue, whereas the free locations appear in white.
In order to wire a differential input (with both inputs adapted on 50 ohms), one must first remove the resistors R3, R6 and R8. Then one has to put 84.5 ohms on R2, 0 ohm on

R5 (use the former R3), 121 ohms on R55 and 50 ohms on R56. Finally, R9 (750 ohms) has to be replaced by 237 ohms and R10 (30.9 ohms) by 10 ohms.



Implementation of the components around the differential amplifier located in the block, bottom left of the MATACQ chip.

Fig. 4.2: Components position

4.2 Interfaces. VME interface

The board is compatible with the A24-D16, A32-D32 and A32-D64 modes. It supports the h08, h09, h0B, h0C, h0D, h0F, h39, h3B, h3D and h3F ADDRESS MODIFIERS, and therefore deals with the accesses in block mode. The sub-addresses are coded over the bits 08 to 15. The A32-D64 mode (MBLT) can be used only for reading.
The base address is given by: switch_address x h10000 (0<switch_address<hFF for A24 D16 and 0<switch_address<hFFFF for A32-D32)
The offset is given by: sub_address x h100 (the sub-address list is given in *4.2.4*)
The complete address is given by: base_address + offset
The VME interrupt (IRQ) is used to signal to the acquisition system the presence of data waiting in the RAM. A block of micro-switches is implemented at the back of the board in order to select on which IRQ line (1 to 7) the interrupt will be sent. It must be released by any writing at the address of the INTERRUPT register, which sets it back to 0. It is anyhow also reset by the START_ACQ command.
The sending of IRQ can be inhibited by the positioning at 1 of the INH_IRQ bit (bit 1 of the CONTROL_REG register).
The presence of waiting data can be equally detected without treating the interruption, but by scanning the presence of a 1 in the same INTERRUPT register. However, it should be avoided because it is a source of noise during the data acquisition.
The reading of the data stored in the RAM is executed by realizing N successive readings at the address of RAM_DATA or by realizing series of readings in block mode at this same address (blocks of 128 16-bit words or 64 32-bit words or 256 64-bit words maximum to comply with the VME standard).

4.2.1 GPIB Interface

The V1729A boards can have an address set between 0 and 29 (decimal).

- Writing

The GPIB commands are carried out by writing a string of bytes in the board situated at the address designated by the rotary switches.
The content of the first byte always corresponds to the sub-address of the order to be executed or of the register to be addressed.
The content of the following bytes correspond to the data. The number of data bytes is free except in the case of a writing to the sub-address hFF which is a read demand (see below). Even in the case of a command, one data byte must always be sent (its value will be ignored in that case).

- Reading

A method of reading by block was implemented to accelerate the reading by GPIB. The reading of an element is thus executed in the following way:

* Writing operation of the 4 bytes (#FF)(#LSB)(#MSB)(#REG) with
- (#FF: byte with value hFF
- (#LSB): byte with value corresponding to the 8 lowest significant bits of the number of bytes to read (nbyte).
- (#MSB): byte with value corresponding to the 8 most significant bits of the number of bytes to read.
- (#REG): byte with value corresponding to the sub-address of the register to read (h0C to read the data stored in the RAM for instance).

* The board then switches to the GPIB "talker" mode and sends nbyte bytes read at the sub-address #REG.
In the general case (outside DATA RAM) nbyte =1.

In GPIB, the 16 bits of data converted by the ADC are read in two consecutive bytes in the order MSByte, LSByte.

- Interruption

At the end of the emptying of the data in the RAM, the V1729A board generates a « Service Request (SRQ)» on the GPIB bus. The board is not compatible with the PARALLEL or SERIAL POLLING protocols. However the GPIB controller can identify the SRQ emitor by sequentially scanning the INTERRUPT registers of the different boards. It is not a source of noise because the acquisition is then already terminated.

Like in VME, the interruption (SRQ) is set back to 0 by any writing at the address of the INTERRUPT register, or by the START_ACQ command. In the same way, the presence of waiting data can equally be detected without treating the interruption, but by scanning the presence of a 1 in the same INTERRUPT register.

- Broadcast Mode.

A writing at the address 30 (decimal) permits realization of a simultaneous writing in all the V1729A boards present on the GPIB bus.

4.2.2 USB Interface.

The V1729A boards are equipped with an USB interface based on the FT245B chip from FTDI. The latter permits accessing the board in USB 2.0 full speed (12Mb/s). A specific data transfer protocol has been developed. It includes the notions of sub-address and interrupt and thus permits using all the board functions as described in this document. The corresponding drivers are available for C language or LabView developments on the http://www.caen.it/nuclear/support.php web site.

4.3 Dealing with the memories

4.3.1 Reading of the data in the RAM; mapping.

During the reading of the MATACQ chips, data is digitized by the 14-bit ADC then transferred in the RAM. The sequence order is always the same : one starts by reading the first cell (upper left-hand) of the matrix, and one finishes with the last one (lower right-

hand), this independently of the position of the trigger and of the stopping point of the acquisition.
One will therefore have to realign the data in relation to the trigger, which was explained in 2.4.2. The channels are treated in parallel, and can be masked individually during the writing in RAM. This implicates that, in the case where NCH channels are validated by the mask (default value = h0F), the data are organized as follows:
A24-D16: 16-bit words by groups of NCH addresses corresponding to the NCH channels (in the order 3 to 0, minus the masked channels).
A32-D32: 32-bit long words: 1st longword: D31..16(CH3); D15..0(CH2); 2nd longword: D31..16(CH1); D15..0(CH0); minus the masked channels
The table below clarifies the arrangement of the words in the RAM (10252 data words maximum).
Following the MATACQ chips data, and this whatever its volume is, one will systematically find a copy of the three registers TRIG_REC, Valp_cp and Vali_cp which permit localizing the trigger position within this data. This permits reading these three registers within the same block as data's and thus diminishing the event readout time. One can check their presence thanks to their bit 15 set to 1.

The data in the table marked with an asterisk (*) are reserved for expert usage.

RAM internal address (HEX)	Type of data (bits 0 to 13)	Bit 14	Bit 15
0000 to NCH-1	First sample (*)	0	0
NCH to 2*(NCH)-1	Vernier	0	0
2*NCH to 3*(NCH)-1	Reset baseline (*)	0	0
3*NCH to 4*(NCH)-1	1st cell	0	0
4*NCH to 5*(NCH)-1	2nd cell	0	0
5*NCH to 6*(NCH)-1	3rd cell	0	0
…	…	0	0
2561*NCH to 2562*(NCH)-1	2559th cell	0	0
2562*NCH to 2563*(NCH)-1	2560th cell (last cell)	0	0
2563*(NCH)	TRIG_REC	0	1
2563*(NCH) + 1	Valp_cp	0	1
2563*(NCH) + 2	Vali_cp	0	1

If the number of columns to read (register NB OF COLS TO READ) chosen is less than 128 (default value), the transfer in RAM will stop when this number will get reached. In such a case, one must be sure that the useful data is located in the first part of the matrix. This is the role of the SYNC_OUT output which signals the passage into the beginning of the matrix. In order to validate it, the ESO bit must be placed at 1 in the control register (see 4.3.2), and one must displace the corresponding strap (S4).

The channel mask register furthermore permits validation of only the utilized channels, which will also permit reduction of the volume of data stored in the RAM. In this case indeed, only the data of the valid channels will be recopied in the RAM, all the while respecting the same storage order of the data.
The access to reading in the RAM is done by secondary addressing. Its internal address is indeed controlled by a 16-bit counter (RAM_INT_ADD) located in the controller placed on the board in the FPGA. This is not to be managed by the external interfaces, the acquisition sequencer generating its own address starting from zero for the writing in the RAM. This counter gets auto-incremented in the course of the addressing. It is systematically reset at zero at the end of the writing cycle, which permits not having to load it when one wants to read all of the memory. However, one can directly have access to an address or a group of addresses given in the RAM by pre-loading it.

Seen from the bus, the reading in the RAM is therefore always done at the same h0C (in GPIB and USB) or h0D (in VME) address.
In GPIB and USB, the 16 bits of data converted by the ADC and stored in the RAM (accessible by reading of 2 bytes at the 0C address) are read in order MSByte, LSByte. Only the 14 LSbits of the data issued from a conversion of the ADC have a significance : the bits from 0 to 13 correspond to the 14 encoded bits. The 2 MSbits are fixed at 0 on the board, and they can be masked during the reading.

4.3.2 Accessing the EEPROM

This version of the board comprises a FLASH EEPROM in order to store data useful for the user, for instance calibration data specific to the board. This EEPROM is a Flash memory AT29LV010A with a depth of 128kbytes. It is shared on the board within two 64-kbyte halves which can be selected thanks to the bit 2 of the TRIGGER_TYPE register (trigger edge). Its main specificity is to require for its writing accesses full pages of 128 bytes, without which data would be lost. Moreover, it contains a software protection filter which requires the use of three keywords before the beginning of each 128-byte page. The loading procedure will thus be the following :

- Load the memory address registers RAM_INT_ADD (at the sub-address 0x0E and 0xOF) with the start address of the first page to download (**the bits 0 to 6 must thus be equal to 0**). This operation resets the hardware part of the software protection filter for the next page (part located in the ALTERA).
- Write at the sub-address 0x2C the 128 data bytes, **always preceeded** by the three following bytes : 0xAA, 0x55, 0xA0 in the same block (there will thus be 131 grouped bytes). Indeed, if two bytes are separated by more than 150µs, the internal loading procedure will be launched.
- Perform a loop reading of the sub-address 0x2D (« data polling ») in order to follow the evolution of the memory internal loading procedure. As long as the latter is not over, the main significant bit (bit 7) will weight the opposite of his last value and the bit 6 will toggle upon every reading. This reading is necessary at least once in order to reset the hardware part of the software protection filter for the next page.
- If the following page is contiguous to the former, send directly the new 131-byte block like described above. Otherwise, first load the address of the new page like previous.

For the memory reading, there is no notion of page or of protection and the procedure is simply the following :

- Load the memory address registers RAM_INT_ADD with the address of the first byte to read.
- Read the required number of bytes at the sub-address 0x2E.

4.4 List of the sub-addresses

The table of the sub-addresses corresponding to the different commands is presented below. A certain number among them are reserved for expert usage. They are indicated by the word « RESERVED » in the « NAME » column. They will not be described in this document and **they should not be used**. In VME, the sub-addresses are coded over the bits A8 to A15, the bits A1 to A7 being unused. For more specific details about the addressing in VME, USB or GPIB, refer to 4.2.

The sub-addresses and the new functionalities of this board have been chosen in such a way to ensure its ascending compatibility with the series of 12-bit dynamic range boards. It is thus directly compatible with the latter at power-up: it can then be driven by default by the same software.
The default values of the registers at power-up allow the board to function “normally” and thus simplify writing the software.

Subadd (HEX)	ACCESS	REG or COM.	NAME	bits of data	Default @ power_on
00*	W/R	Reg	INTERRUPT	2	0
01*	W/R	Reg	FP_FREQUENCY	6	1
02*	R	Reg	FPGA VERSION	8	-
03*	W/R	Reg	MODE_REGISTER	3	0
04	R	Reg	EVOLUTION of the FPGA VERSION	8	-
08	W	Com	RESET BOARD	NO	-
09	W	Com	LOAD TRIGGER THRESHOLD DAC	NO	-
0A**	W	Reg	TRIGGER THRESHOLD DAC ALL CHANNELS TOGETHER (LSB->GPIB or USB, word->VME)	8 or 12	0
0B**	W	Reg	TRIGGER THRESHOLD DAC MSB (half byte->GPIB or USB)	4	0
0C**	R	Reg	RAM DATA MSB + LSB -> GPIB or USB	8	-
0D**	R	Reg	RAM DATA ->VME	16	-
0E	W/R	Reg	RAM_INT_ADD LSB	8	0
0F	W/R	Reg	RAM_INT_ADD MSB	8	0
10	W/R	Reg	MAT CTRL REGISTER LSB	8	0
11	W/R	Reg	MAT CTRL REGISTER MSB	8	0
12	W	Com	RESERVED	NO	-
13	W	Com	RESERVED	NO	-
14	W	Com	RESERVED	NO	-
15	W	Com	RESERVED	NO	-
16	W	Com	RESERVED	NO	-
17	W	Com	START ACQUISITION	NO	-
18	W/R	Reg	PRETRIG LSB	8	0
19	W/R	Reg	PRETRIG MSB	8	40
1A	W/R	Reg	POSTTRIG LSB	8	64
1B	W/R	Reg	POSTTRIG MSB	8	0
1C	W	Com	SOFTWARE TRIGGER	NO	-
1D	W/R	Reg	TRIGGER TYPE	8	0
1E	W/R	Reg	TRIGGER CHANNEL SOURCE	4	0
20	R	Reg	TRIG_REC	8	-
21	W/R	Reg	FAST READ MODES	2	0
22	W/R	Reg	NB OF COLS TO READ	8	128

23	W/R	Reg	CHANNEL MASKS	4	h0F
24	W/R	Reg	RESERVED	8	64
26	R	Reg	Valp_cp REGISTER	5	
27	R	Reg	Vali_cp REGISTER	5	
28	W/R	Reg	TRIGGER THRESHOLD DAC ch0 (LSB->GPIB or USB, word->VME)	8 or 16	2048
29	W/R	Reg	TRIGGER THRESHOLD DAC ch1 (LSB->GPIB or USB, word->VME)	8 or 16	2048
2A	W/R	Reg	TRIGGER THRESHOLD DAC ch2 (LSB->GPIB or USB, word->VME)	8 or 16	2048
2B	W/R	Reg	TRIGGER THRESHOLD DAC ch3 (LSB->GPIB or USB, word->VME)	8 or 16	2048
2C	W	Mem	User EEPROM (128kBytes) : Write access	8	
2D	R	Mem	User EEPROM (128kBytes) : Poll access	8	
2E	R	Mem	User EEPROM (128kBytes) : Read access	8	
30	W/R	Reg	POST STOP LATENCY	8	4
31	W/R	Reg	POST LATENCY PRETRIG	8	1
34	W/R	Reg	NUMBER OF CHANNELS	3	4
38	W/R	Reg	RATE_REG	1	0
39	R	Reg	TRIG_COUNT LSB	8	
3A	R	Reg	TRIG_COUNT MSB	8	
3B	R	Reg	TRIG_RATE LSB	8	
3C	R	Reg	TRIG_RATE MSB	8	
3D	R	Reg	TRIG_COUNT + TRIG_RATE Block access	4x8	
FF*	W	Reg	NB OF BYTES TO READ IN BLOCK MODE (GPIB)	24 (3x8)	1

* also decoded with the sub-address MSB set to 1 in order to ensure the ascending compatibility with the softwares developed for former versions of the boards.
** mind the different use in VME and GPIB/USB.

The sub-addresses are organized by type. For more detail on their specific use in VME, USB or GPIB, refer to 4.2.

The functions of these different commands and registers are described below:

- INTERRUPT: bit 0 of this register memorizes the arrival of the interruption which signals the end of the acquisition phase. The INTERRUPT signal is forwarded towards the acquisition buses, but it can also be read here. It is also here that it must be released and reset at zero by a simple write access. It is anyhow reset by the START_ACQ command.

Bit 1 of this register flags a potential overflow of the event-buffer FIFO linked to accesses on the data bus during the data transfer between the MATACQ chips and the RAM. Finding this bit set at 1 after an interruption would make the event non valid.

Bits	*Function*
0	Val = 0 => end of acquisition interruption not yet sent Val = 1 => end of acquisition interruption already sent
1	Val = 0 => OK Val =1 => there was an overflow of the event-buffer during the last event transfer. The event is not valid.

- FP_FREQUENCY: this 6-bit register permits fixing the Fp period. initialized at 1

Bits	*Function*
0-5	Val = 1 => Fsample = 2GHz. Val = 2 => Fsample = 1GHz. Val = 4 => Fsample = 500MHz. Val = 5 => Fsample = 400MHz. Val = 10 => Fsample = 200MHz. Val = 20 => Fsample = 100MHz. Val = 40 => Fsample = 50MHz.

FPGA VERSION : this 8-bit read-only register permits reading the version number of the FPGA. The 4 MSbits give the type of board and the 4 LSbits the version number of the firmware stored in the PROM. The code corresponding to the V1729A board is F, which gives a root number of hF0 for FPGA VERSION.

MODE_REGISTER : 2-bit register. The two first bits concern the VME interrupt and the data readout mode. Bit 2 permits automatically restarting (see 2.3.2) the acquisition after the reading in the RAM (see 4.3.1) of the first of TRIG_REC, Valp_cp and Vali_cp.

Bits	Nom	Default	Function
0	EN_VME_IRQ	0	This bit permits enabling (1) or not (0) the output of the interruption tagging the end of the acquisition towards the VME bus.
1	14BIT_MODE	0	If this bit is set at 0, the board outputs its data over 12 bits in a way compatible with the software versions developed for the former 12-bit boards. If set at 1, data is over 14 bits.
2	AUTO_RESTART_ACQ	0	Val = 0 => Normal mode for starting the acquisition (via the START_ACQUISITION command). Val = 1 => Automatic restart of the acquisition at the end of the RAM readout.

EVOLUTION of the FPGA VERSION : this 8-bit read-only register permits reading the evolution number of the FPGA version.

- RESET BOARD : reset of the board. Restores idle state. Does not modify the values loaded in the different registers.
- LOAD TRIGGER THRESHOLD DAC : permits transfer of the pre-loaded value in the register of the DACs towards the analog converter itself.
- START ACQUISITION : launches the data acquisition and resets the INTERRUPT register at the sub-address h80. When this is finished, the INTERRUPT signal will be validated, transmitted towards the bus interfaces, and become available at the sub-address h80.
- SOFTWARE TRIGGER : permits generation of a trigger coming from a bus interface.
- TRIGGER THRESHOLD DAC : common pre-loading register of the DACs. This 12-bit register covers the range from –1V (000) to +1V (FFF). By USB or GPIB, one has access to the MSBs and LSBs via 2 distinct sub-addresses. The access is necessarily made in the order MSB (0B) then LSB (0A). By VME, the access is made

via a single sub-address (0A). After loading of this register, one must transfer the value in the analog converter via the LOAD_TRIGGER THRESHOLD DAC (09) command.

- RAM DATA : this is the memory where the data is stored. As above, the access to the data is made differently in GPIB and in VME (see NB OF BYTES TO READ IN BLOCK MODE). The addressing is indirect, the internal address of the RAM being defined by the RAM_INT_ADD counter located in the ALTERA. Data readout thus always makes use of the single 0D address in VME and of the 0E and 0F addresses in GPIB.
- RAM_INT_ADD : this 16-bit counter fixes the internal address of the RAM for the bus access in progress. It is set back to zero by the RESET_BOARD command and by the interruption at the end of the acquisition phase. For a direct access to an address or a given group of addresses, one must pre-load it.
- MAT CTRL REGISTER : this is a control register for the acquisition parameters. It covers 11 useful bits. The bits followed by an asterisk are reserved and must be left at zero.

Bits	Name	Default	Function
0	BWL	0	Regulates the bandwidth of the input amplifiers with BWL1
1	BWL1	0	Regulates the bandwidth of the input amplifiers with BWL
2	EBP	0	At 1, authorizes the bypass of the input signal towards the ADC
3	ELD*	-	Reserved
4	ENVDLL*	0	Reserved
5	EIR*	0	Reserved
6	EPR	0	At 1, forces the permanent supply of the reading amplifiers
7	EPW	0	At 1, forces the permanent supply of the writing amplifiers
8	ESO	0	At 1, authorizes the SYNC_OUT signal to be output from the board (thanks to the corresponding strap S4)
9	ISA	0	At 1, inhibits the START_ACQUISITION command.
10	IRQP	0	At 1, inhibits the automatical RQP before the acquisition.

- PRETRIG : this 16-bit register fixes the delay in periods of Fp between the START ACQUISITION and the internal authorization to validate a trigger, whatever the source of the latter. For proper functioning, it must be fixed at a minimum of 5000 for an Fp frequency of 50MHz and at 10000 for a frequency of 100MHz. By default, its value is 10240.
- POSTTRIG : this 16-bit register fixes the delay in periods of Fp between the trigger and the stopping of the acquisition. It permits in practice choosing the useful position of the signal in the window of 2560 cells. By default, its value is 64.
- TRIGGER TYPE : this 6-bit register fixes the trigger's source and mode. The bits 6 and 7 permit dealing with the situation where a few cards have been interconnected to work together. **Warning**: bit 2 has two different meanings.

Bits	*Function*
0-1	Val = 0 => SOFTWARE TRIGGER Val = 1 => trigger on discriminator (threshold fixed by the DAC) Val = 2 => external trigger from the TRIG_EXT input Val = 3 => logic "OR" of SOFTWARE TRIGGER and trigger on discriminator
2	Val = 0 => rising edge or selection of the lowest half of user EEPROM

	Val = 1 => falling edge or selection of the highest half of user EEPROM
3	Val = 0 => Inhibites random internal trigger. Val = 1 => Authorizes random internal trigger.
4	Val = 0 => one uses the Trigger normally. Val = 1 => one uses the external Trigger directly and without masking.
5	Bit = EnValidTrig. Val = 0 => the Trigger directly launches the readout. Val = 1 => the Trigger has to be validated by the EN_EXT_TRIG input in order to launch the readout.
6	Selection of the reset mode of the BUSY signal: Val = 0 => one takes EN_EXT_TRIG into account. Val = 1 => one ignores EN_EXT_TRIG.
7	Permits inhibiting the BUSY signal: Val = 0 => the BUSY signal is performing in a usual way. Val = 1 => the BUSY signal is pulled at zero (inactive).

- TRIGGER_CHANNEL_SOURCE : this 4-bit register fixes the channel(s) from which the discriminators will release the trigger. More than one channel can be validated at the same time because one realizes a logic « OR » of the outputs of the discriminators in the controller.

Bits	*Function*
0	Val = 0 => Disables Trigger on channel 0. Val = 1 => Enables Trigger on channel 0.
1	Val = 0 => Disables Trigger on channel 1. Val = 1 => Enables Trigger on channel 1.
2	Val = 0 => Disables Trigger on channel 2. Val = 1 => Enables Trigger on channel 2.
3	Val = 0 => Disables Trigger on channel 3. Val = 1 => Enables Trigger on channel 3.

  - TRIG_REC : this 8-bit register gives the distance between the column where one finds the column pointer at the arrival time of the synchronous trigger and the last column (128). It permits in practice to roughly date the useful signal to the nearest clock rising edge. This dating will be refined with greater precision by the utilization of the vernier.
  - FAST READ MODES : this 2-bit register permits realization of a faster reading of the MATACQ chips in some specific applications.

Bits	*Function*
0	Val = 0 => sequence with reading of TRIG_REC (normal) Val = 1 => sequence without reading of TRIG_REC (short)
1	Val = 0 => sequence departing from the first column (normal) Val = 1 => sequence departing from the STOP (possible reduced readout depth)

  - NB OF COLS TO READ : this 8-bit register gives the number of columns that one wants to read in the matrix. The number of columns can be fixed between 0 et 128. The stored value is by default 128, which corresponds to the whole matrix.
  - CHANNEL MASKS : each one of the 4 bits in this register individually validates a channel on the board. For this, they must be set at 1. At zero, the corresponding channel is masked and its data will not be recorded in the RAM. Caution : this modifies the format of the frame stored in the RAM (see 4.3).
- Valp_cp & Vali_cp REGISTERS : these registers have to be used only for the sampling frequencies lower or equal to 500MHz, when the rotating maks Valp and Vali are used themselves. They permit locating the trigger in this case. They must be read out after TRIG_REC. They give the number of the line where one finds the first mask bit at 1 for each of the two registers (line number between 0 and 19). .
  - TRIGGER THRESHOLD DAC Ch# : individual pre-loading registers of the DACs. These 12-bit registers cover the range from –1V (000) to +1V (FFF). By USB or GPIB, one has access to the MSBs and LSBs via 2 distinct sub-addresses. The access is necessarily made in the order MSB (0B) then LSB (28 to 2A). By VME, the access is made via a single sub-address (28 to 2A).
  - User EEPROM access : see 4.3.2.

- POST STOP LATENCY : this register permits the programming with steps of 2.5µs of the time during which the board waits for the validation signal in the mode where the latter is used to launch the readout of the MATACQ chips towards the RAM. The default value is of 10µs whereas the minimum one is of 2.5µs.

- POST LATENCY PRETRIG : this register fixes with steps of 2.5µs the time to wait before enabling the trigger again consequently to the absence of the validation signal during the window fixed by POST_STOP_LATENCY. The default value, which is set to be the minimum one, is of 2.5µs.
- NUMBER OF CHANNELS : this register sets over 3 bits the number of acquisition channels of the board.

Bits	*Function*
0-2	Val = 1 => 1 channel of 10240 samples (0-1-2-3) Val = 2 => 2 channels of 5120 samples each (0-1 et 2-3) Val = 4 => 4 channels of 2560 samples each Any other value => 4 channels of 2560 samples each

- RATE_REG : this register permits activating or not the counting of the trigger rate.

Bits	*Function*
0	Val = 0 => trigger rate monitor non active Val = 1 => trigger rate monitor active

- TRIG_COUNT : this register counts the number of triggers produced in the current trigger conditions defined for the board. It works up to 200MHz, starts upon TRIGA and stops:
  - either upon the reading of any of the two counters,
  - or when any of them saturates.

It is possible to read the four bytes of the two counting registers in block mode at the sub-address 0x3D (equivalent to the order 0x39 to 0x3C) and thus to gain a lot of time in USB for instance.

- NB OF BYTES TO READ IN BLOCK MODE : for the readings in block mode by GPIB solely, this 16-bit register permits fixing the number of bytes contained in the block. In order to simplify the accesses by reading to the RAM, one will send as in the reading order 4 bytes of data : the 1st with hFF, the 2nd and the 3rd with respectively the LSBs then the MSBs of the number of bytes to read, and finally the 4th with the sub-address h0C for the RAM. The MSBs then the LSBs will then be sent successively. Do not forget to double the number of data to read in the RAM when passing from the number of words to the number of bytes.

4.5 Synopsis of the board

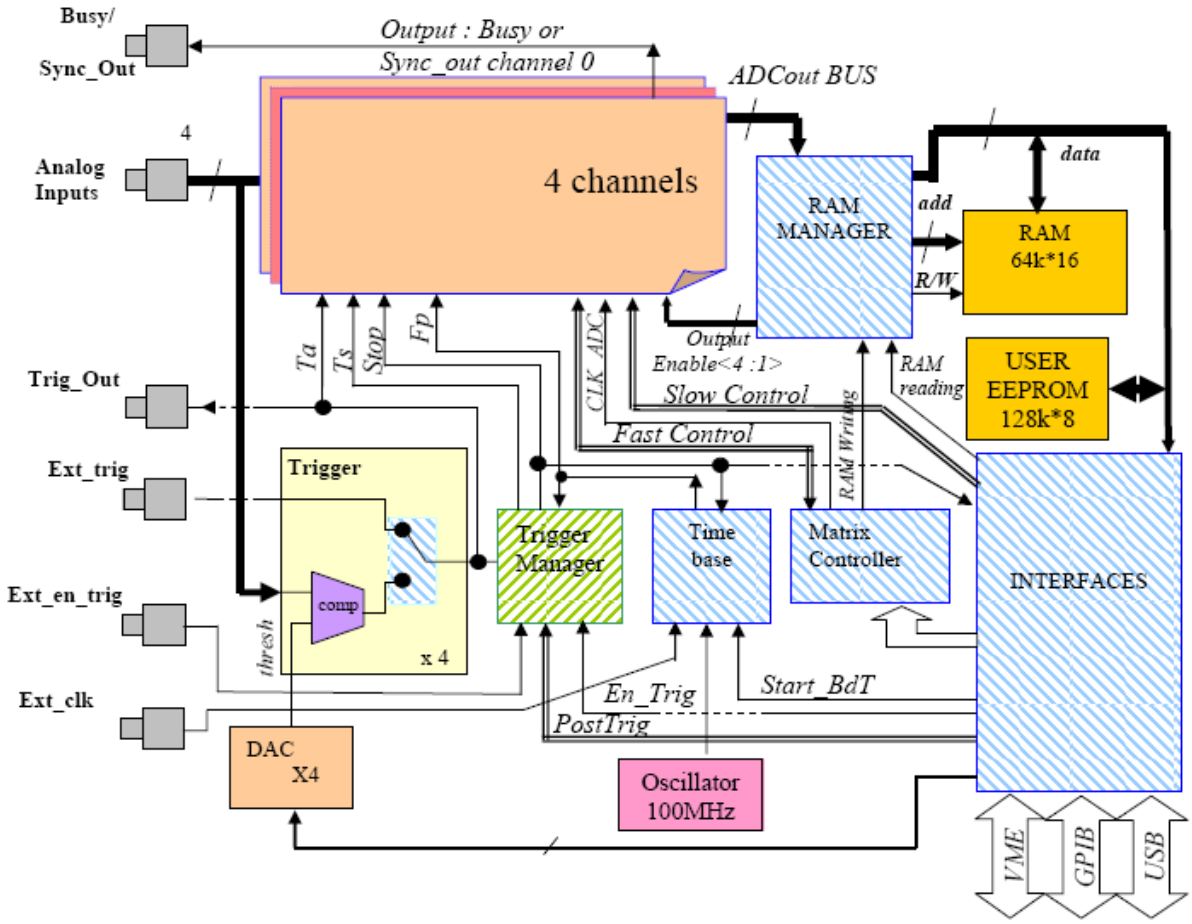


Fig. 4.1: synopsis of the V1729A board

The architecture of the V1729A board (Fig4.1) is modular. This architecture as well as the components used were selected so as to minimize the costs of conception and production of the board. The board is principally made up of six blocks :

- The 4 channels of acquisition and fast digitization (synopsis of a channel in Fig 4.2).
- The management of the trigger.
- The management of the clocks.
- The slower readout of the MATACQ chips.
- The management of writing and of re-reading the digital memory (RAM).
- The interfacing with the acquisition system and the management of the user EEPROM.

The trigger management part is integrated in a dedicated CPLD. The last four blocks (except the RAM itself) as well as the digital part of the trigger system are integrated in a single programmable component (FPGA) with wide possibilities. This considerably reduces the costs of production and may still permit an easy upgrading of the system in the future if necessary.
An E2PROM also permits storing parameters specific to the board from the acquisition software, for instance in the wake of a calibration.

The different logical level translations present on the board are not represented in the synopsis.

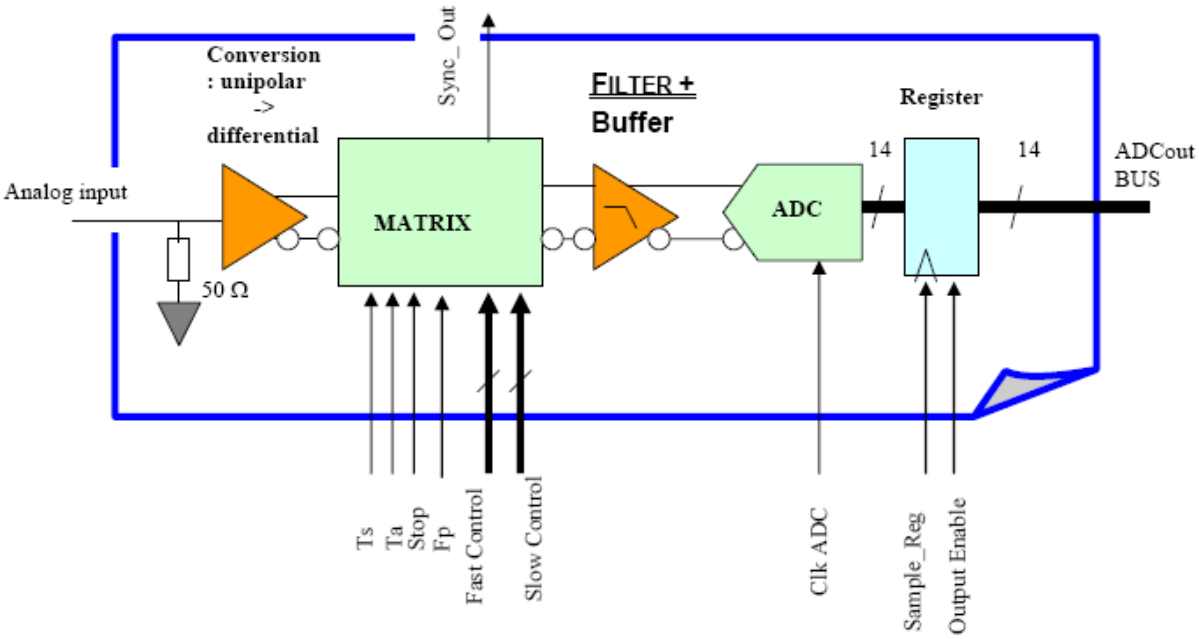


Fig. 4.2: Synopsis of an acquisition channel on the board

The elementary block of the analog acquisition is represented in Fig 4.1. It includes :

- The 50-Ohm adaptation of the input.
- A large bandwidth amplifier making it possible to feed the MATACQ chip in differential.
- The MATACQ chip.
- A bandwidth limiter filter.
- The 14bit-5MHz ADC, differential.
- A register allowing the multiplexing of the data coming from the different channels towards the RAM.

5. Specifications and performances

The following table summarizes the principal specifications and performances of the V1729A board.

Input analog signals	
Number of channels	4
Input impedance	50 Ohms
Dynamic Range	± 1V
Bandwidth	300MHz
Noise/signal ratio	13.5 bits RMS (noise =175 µV RMS)
Harmonic distorsion	< -60dB for sinusoidal input at 25MHz
LSB (digitization step)	0.125 mV
Integral Non Linearity	< 1 per mil
Differential Non Linearity	< 0.05 per mil
Relative gain between channels	< ±1%.
Sampling	
Max Frequency	2GS/s
Min Frequency	50MS/s
Time precision in a single channel	15ps RMS typical
Time precision between two channels	20ps RMS typical
Depth per channel	2560 points (of which 2520 are usable)
Trigger	
Threshold setting dynamic range	± 1V
Threshold setting step	0.5mV
Time precision	50ps RMS typical*
Analog to Digital Conversion	
Conversion frequency	5MHz
Resolution	14 bits
Time to empty the matrices into the RAM	675µs
Acquisition	
Acquisition rate (VME)	Up to 800 acquisitions/s over 4 full channels
Acquisition rate (GPIB)	Up to 100 acquisitions/s over 4 full channels
Acquisition rate (USB)	Up to 50 acquisitions/s over 4 full channels
Front Panel Signals (TRIG_OUT, SYNC_OUT, TRIG_EXT)	
NIM Standard (negative logics) :	
Input Impedance (TRIG_EXT)	50 Ohms
Lower max level (logic 1)	-0.6V
Upper min level (logic 0)	-0.2V
Power Supplies	
Min voltage on « +5V »	4.5V
Min voltage on « +12V »	6.5V
Min voltage on « -12V »	-6.5V
Consumption on +5V	1.5A when idle, 3A max (varies with acquisition rate)
Consumption on +12V	typ 350mA
Consumption on -12V	typ 150mA

* includes both sampling and trigger precisions.

5.1 Front panel

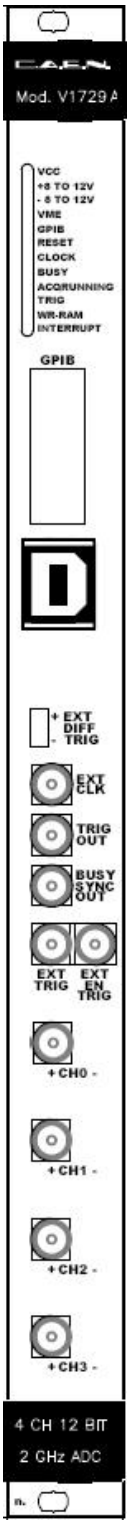


Fig. 5.1: V1729A Front Panel

6. Bibliography

[1] E. Delagnes, D. Breton **, Echantillonneur analogique rapide à grande profondeur mémoire.** French patent n° **01 05607** from April 26th 2001. US Patent **6,859,375** from February 22nd 2005**: Fast analog sampler with great memory depth**.

7. Appendix - Using the rotating masks

7.1 Working principle

The MATACQ chip (see figure 7.1) is an analog sampling matrix made of 20 lines and 128 columns. The write pointer propagates vertically within each column and shifts from left to right column by column at the frequency of the clock delivered to the circuit. At 1 or 2 GS/s, all the 20 points of the column are written sequentially. In order to reduce the sampling frequency, rotating masks have to be used. They permit writing into only one out of N cells, N being all the possible dividers of 20 (2, 4, 5, 10, 20). There are two rotating masks, each in charge of one half (left or right) of the matrix. The reason therefore is to avoid having a fast mask transition during the writing phase. Transitions will then be slow and non perturbative, and occur in areas located far away from the write pointer.
This section describes an example of recording througout the whole depth of the matrix while using the rotating masks. The division factor chosen is 4 (used for a 500MS/s sampling). P represents the write pointer. The principle is identical for all the other factors listed hereabove. The numbers inside the matrix represent the ordered number of the samples with the time. For the full filling up, one will have to wait in this example for 4 laps of the matrix. Then the pointer comes back to the same cells until the end of the acquisition.

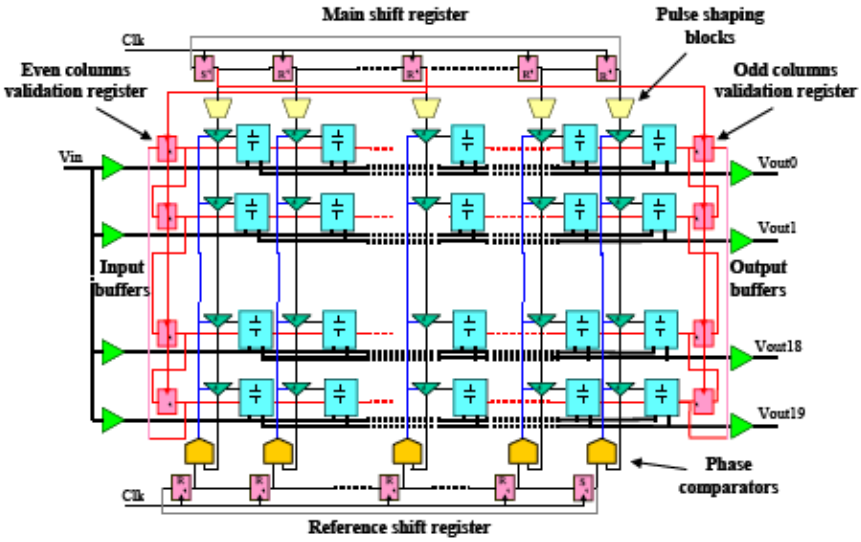


Fig. 7.1: working principle of the board (patented)

The shift register in charge of controlling the left side of the matrix is called Valp, while that in charge of the right side is called Vali. Vali is shifted whenever the write pointer passes through the 2nd column, whereas Valp is shifted whenever the write pointer passes through the 66th column. The right side of the matrix is thus always shifted by one line to the bottom (as shown on figure 7.2 for instance) when the write pointer crosses between the two halves, which implies **a time shift of 0.5ns between 500MS/s and 100MS/s and of 1ns at 50MS/s** when one passes from the 64th to the 65th column. This time shift has to be taken into account to calculate the actual sampling times in the cells. The propagation time throughout the columns is indeed of 10ns between 500MS/s

and 100MS/s and of 20ns at 50MS/s. Masks are automatically loaded into the MATACQ chips at the beginning of each acquisition depending on the chosen sampling frequency. In order to make this choice, one has to load the value of the division factor with respect to 2GS/s into the FP_FREQUENCY register at the sub-address 0x81 (1 for 2GS/s, 2 for 1GS/s, 4 for 500MS/s, …). During the reading of the matrix, and this whatever the sampling frequency, the samples are usually read and stored column by column into the RAM, starting from the top of the first column. There are thus not anymore sorted in the order in which they were sampled if the masks have been used. Consequently, they will have to be reordered. **But the pedestal subtraction has to be performed first, because pedestals only depend on the geographical position inside the matrix.** Caution : the last recorded line is located at the very bottom of the left half of the matrix, but N-1 lines higher on the right half. The difficulty which then arises is to reposition the trigger with respect to data. Therefore, the board permits accessing the status of the two mask registers at the trigger arrival time. Information about Valp is available at sub-address 0x26 and about Vali at sub-address 0x27. The two decimal values present give the distance between the first bit at 1 with respect to the first line (which means 0 for the latter, and 19 for the bottommost) for each of the two registers (they may be different). From these two values, and those of the vernier and the trigger column, one can precisely localise the trigger. Caution : the vernier used alone in the trigger column in the usual way may fall on a cell which wasn't sampled at that precise time. It is the very role of Valp and Vali to permit interpolating between the two closest **real** samples. Actually, this rotating mask system has the great advantage of not deteriorating the sampling time precision when one wants to decrease the sampling frequency. On the other hand, it is clear that the time shift when crossing between the two halves of the matrix which is not bothering for a temporal use of the recorded signal because the sampling instants are perfectly defined, may become a problem if one wants to perform a Fourier transform of said signal. For a precise FFT, it will be necessary to perform at least a third order interpolation over 3 real points in order to reconstruct with a sufficient precision the position of each equidistant missing point. Another solution consists in using a Fourier transform with non equidistant points (floating point abscissa).

7.1.1 Example of working at 500 MS/s

Valp	1	2	3	…	62	63	64	65	66	67	…	126	127	128	Vali
1	P														1
0															0
0															0
0															0
1															1
0															0
0															0
0															0
1															1
0															0
0															0
0															0
1															1
0															0
0															0
0															0
1															1
0															0
0															0
0															0

Fig. 7.2: state of the matrix at the beginning

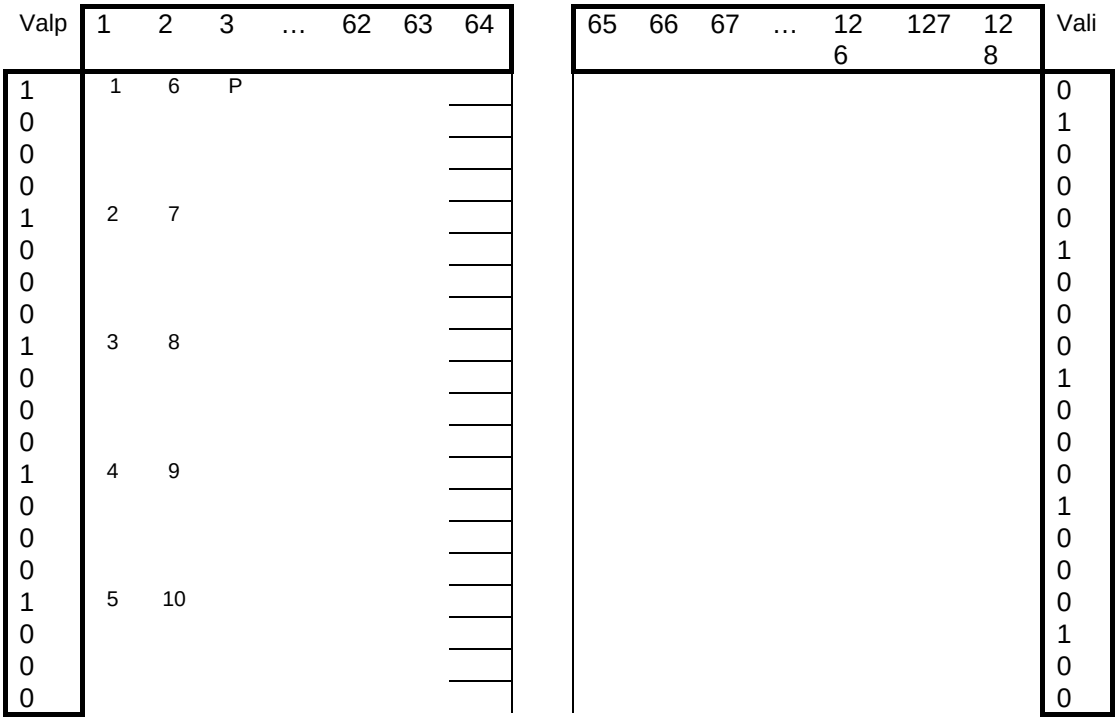


Fig. 7.3: state of the matrix after the crossing of column 2

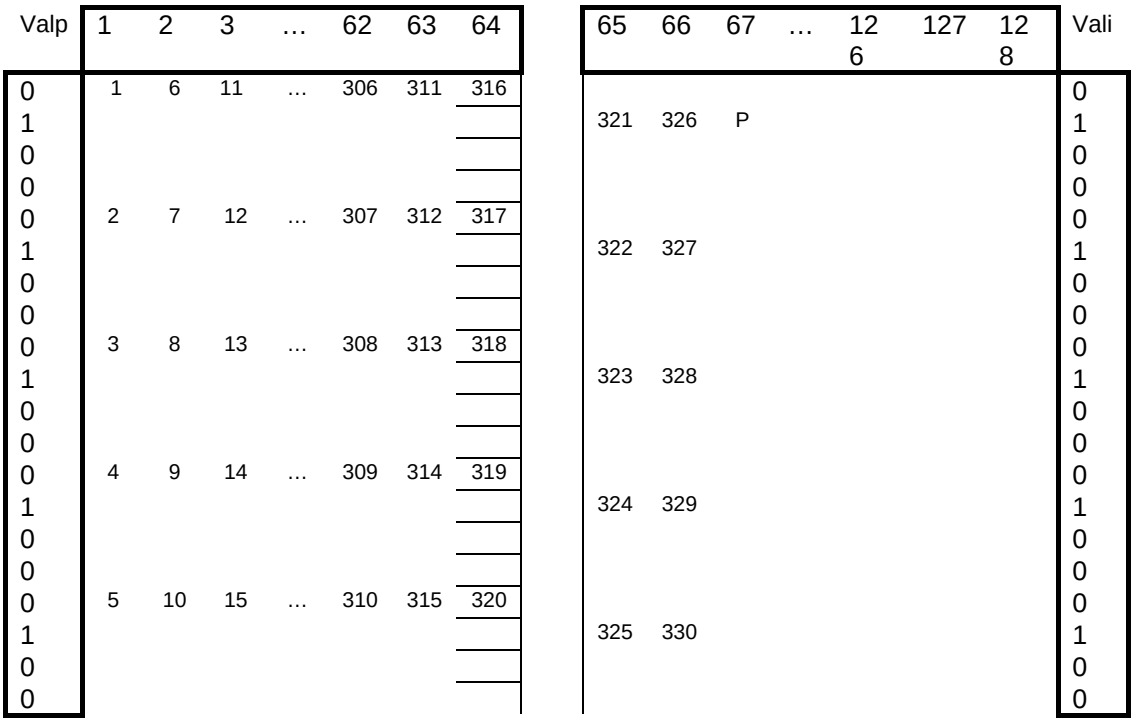


Fig. 7.4: state of the matrix after the crossing of column 66

Valp	1	2	3	…	62	63	64	65	66	67	…	126	127	128	Vali
0	1	6	11	…	306	311	316								0
1	641	646	P					321	326	331	…	626	631	636	0
0															1
0															0
0	2	7	12	…	307	312	317								0
1	642	647						322	327	332	…	627	632	637	0
0															1
0															0
0	3	8	13	…	308	313	318								0
1	643	648						323	328	333	…	628	633	638	0
0															1
0															0
0	4	9	14	…	309	314	319								0
1	644	649						324	329	334	…	629	634	639	0
0															1
0															0
0	5	10	15	…	310	315	320								0
1	645	650						325	330	335	…	630	635	640	0
0															1
0															0

Fig. 7.5: state of the matrix after the 2nd crossing of column 2

Valp	1	2	3	…	62	63	64	65	66	67	…	126	127	128	Vali
0	1	6	11	…	306	311	316								0
0	641	646	651	…	946	951	956	321	326	331	…	626	631	636	0
1								961	966	P					1
0															0
0	2	7	12	…	307	312	317								0
0	642	647	652	…	947	952	957	322	327	332	…	627	632	637	0
1								962	967						1
0															0
0	3	8	13	…	308	313	318								0
0	643	648	653	…	948	953	958	323	328	333	…	628	633	638	0
1								963	968						1
0															0
0	4	9	14	…	309	314	319								0
0	644	649	654	…	949	954	959	324	329	334	…	629	634	639	0
1								964	969						1
0															0
0	5	10	15	…	310	315	320								0
0	645	650	655	…	950	955	960	325	330	335	…	630	635	640	0
1								965	970						1
0															0

Fig. 7.6: state of the matrix after the 2nd crossing of column 66

Valp	1	2	3	…	62	63	64	65	66	67	…	126	127	128	Vali
0	1	6	11	…	306	311	316								1
0	641	646	651	…	946	951	956	321	326	331	…	626	631	636	0
0	1281	1286	1291	…	1586	1591	1596	961	966	971	…	1266	1271	1276	0
1	1921	1926	P					1601	1606	1611	…	1906	1911	1916	0
0	2	7	12	…	307	312	317								1
0	642	647	652	…	947	952	957	322	327	332	…	627	632	637	0
0	1282	1287	1292	…	1587	1592	1597	962	967	972	…	1267	1272	1277	0
1	1922	1927						1602	1607	1612	…	1907	1912	1917	0
0	3	8	13	…	308	313	318								1
0	643	648	653	…	948	953	958	323	328	333	…	628	633	638	0
0	1283	1288	1293	…	1588	1593	1598	963	968	973	…	1268	1273	1278	0
1	1923	1928						1603	1608	1613	…	1908	1913	1918	0
0	4	9	14	…	309	314	319								1
0	644	649	654	…	949	954	959	324	329	334	…	629	634	639	0
0	1284	1289	1294	…	1589	1594	1599	964	969	974	…	1269	1274	1279	0
1	1924	1929						1604	1609	1614	…	1909	1914	1919	0
0	5	10	15	…	310	315	320								1
0	645	650	655	…	950	955	960	325	330	335	…	630	635	640	0
0	1285	1290	1295	…	1590	1595	1600	965	970	975	…	1270	1275	1280	0
1	1925	1930						1605	1610	1615	…	1910	1915	1920	0

Fig. 7.7: state of the matrix after the 4th crossing of column 2

Valp	1	2	3	…	62	63	64	65	66	67	…	126	127	128	Vali
1	1	6	11	…	306	311	316	2241	2246	2251	…	2546	2551	2556	1
0	641	646	651	…	946	951	956	321	326	331	…	626	631	636	0
0	1281	1286	1291	…	1586	1591	1596	961	966	971	…	1266	1271	1276	0
0	1921	1926	1931	…	2226	2231	2236	1601	1606	1611	…	1906	1911	1916	0
1	2	7	12	…	307	312	317	2242	2247	2252	…	2547	2552	2557	1
0	642	647	652	…	947	952	957	322	327	332	…	627	632	637	0
0	1282	1287	1292	…	1587	1592	1597	962	967	972	…	1267	1272	1277	0
0	1922	1927	1932	…	2227	2232	2237	1602	1607	1612	…	1907	1912	1917	0
1	3	8	13	…	308	313	318	2243	2248	2253	…	2548	2553	2558	1
0	643	648	653	…	948	953	958	323	328	333	…	628	633	638	0
0	1283	1288	1293	…	1588	1593	1598	963	968	973	…	1268	1273	1278	0
0	1923	1928	1933	…	2228	2233	2238	1603	1608	1613	…	1908	1913	1918	0
1	4	9	14	…	309	314	319	2244	2249	2254	…	2549	2554	2559	1
0	644	649	654	…	949	954	959	324	329	334	…	629	634	639	0
0	1284	1289	1294	…	1589	1594	1599	964	969	974	…	1269	1274	1279	0
0	1924	1929	1934	…	2229	2234	2239	1604	1609	1614	…	1909	1914	1919	0
1	5	10	15	…	310	315	320	2245	2250	2255	…	2550	2555	2560	1
0	645	650	655	…	950	955	960	325	330	335	…	630	635	640	0
0	1285	1290	1295	…	1590	1595	1600	965	970	975	…	1270	1275	1280	0
0	1925	1930	1935	…	2230	2235	2240	1605	1610	1615	…	1910	1915	1920	0

Fig. 7.8: state of the matrix at the end of the filling up.